EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Andrew T Zidel, Reg. No. 45,256 on 06/30/2009.

3. The following claim had been amended:

This listing of claim will replace all prior versions and listings of claims in the application:

1. (currently amended) A method of managing processor tasks in a multi-processor computing system, comprising:

storing the processor tasks in a shared memory that is accessible by a plurality of processing units of the multi-processor computing system;

permitting the processing units to determine which of the processor tasks should be executed based on priorities of the processor tasks, wherein the processor tasks that are executed are copied from the shared memory to the local memory of a processing unit;

copying a task table from the shared memory to the local memory of a processing unit, the task table including a task table entry associated with each of the processor tasks;

modifying the task table entry of a selected one of the processor tasks;

linking at least some of the task table entries together to achieve at least one list of the processor tasks to be invoked in hierarchical order; and

copying the task table from the local memory of a processing unit to the shared memory to include the modified task table entry in the task table;

wherein each of the task table entries includes at least one of: (i) an indication as to whether the associated processor task is ready to be executed by one or more of the processing units; (ii) an indication as to a priority level of the associated processor task; (iii) a pointer to a previous task table entry in a list of task table entries (a previous pointer); and (iv) a pointer to a next task table entry in the list of task table entries.

2. (cancelled)

3. (original) The method of claim 1, wherein the processing units comprise a main processing unit and a plurality of sub-processing units and the sub-processing units access the processor tasks in the shared memory.

4. (currently amended) A method of managing processor tasks in a multi-processor computing system, comprising:

storing the processor tasks in a shared memory that is accessible by a plurality of processing units of the multi-processor computing system;

storing a task table in the shared memory, the task table including a task table entry associated with each of the processor tasks;

linking at least some of the task table entries together to achieve at least one list of the processor tasks to be invoked in hierarchical order; and

permitting the processing units to use the task table to determine which of the processor tasks should be executed in accordance with the list of processor tasks, wherein the processor tasks that are executed are copied from the shared memory to a local memory of a given one of the processing units;

copying the task table from the shared memory to the local memory of the given processing unit;

modifying a selected one of the task table entries; and

copying the task table from the local memory of the processing unit to the shared memory to include the modified task table entry;

wherein each of the task table entries includes at least one of: (i) an indication as to whether the associated processor task is ready to be executed by one or more of the processing units; (ii) an indication as to a priority level of the associated processor task; (iii) a pointer to a previous task table entry in a list of task table entries (a previous pointer); and (iv) a pointer to a next task table entry in the list of task table entries.

5-6. (cancelled)

7. (previously presented) The method of claim 4, further comprising:

storing a task queue in the shared memory, the task queue including at least one of a head pointer and a tail pointer, the head pointer providing an indication of a first one of the processor

tasks in the list of processor tasks, and the tail pointer providing an indication of a last one of the processor tasks in the list of processor tasks; and

permitting the processing units to use the task table and the task queue to determine which of the processor tasks should be executed in accordance with the list of processor tasks.

8. (cancelled)

9. (original) The method of claim 7, further comprising:

linking respective groups of the task table entries together to produce respective lists of processor tasks, each list being in hierarchical order; and

providing that the task queue includes respective task queue entries, each entry including at least one of a head pointer and a tail pointer for each of the lists of processor tasks.

10. (original) The method of claim 9, wherein:

each of the respective lists are associated with processor tasks of a common priority level; and

the task queue includes a task queue entry for each of a plurality of priority levels of the processor tasks.

11. (original) The method of claim 7, wherein the plurality of processing units includes a plurality of sub-processing units, each of the sub-processing units having local memory, further comprising:

copying the task queue and the task table from the shared memory into the local memory of a given one of the sub-processing units;

searching the task queue for the head pointer to a given one of the processor tasks that is ready to be invoked; and

copying the given processor task from the shared memory to the local memory of the given sub-processing unit for execution.

12. (original) The method of claim 11, wherein the step of searching the task queue includes searching for the head pointer to a highest priority level one of the processor tasks that is ready to be invoked.

13. (previously presented) The method of claim 11, further comprising: removing the given processor task from the list of processor tasks.

14. (original) The method of claim 13, wherein:

each of the task table entries includes a pointer to a next task table entry; and

the removal step includes using the next pointer of the given task table entry to change the head pointer to identify the new first processor task as being ready to be next invoked.

15. (original) The method of claim 13, wherein:

each of the task table entries includes a pointer to a previous task table entry; and

the method further includes modifying the previous pointer of the last task table entry of the list to point to the task table entry associated with the new first processor task of the list.

16. (original) The method of claim 11, wherein:

each of the task table entries includes an indication as to whether the associated processor task is READY to be executed or is RUNNING on one or more of the sub-processing units; and

the method further includes modifying the given task table entry to indicate that the given processor task is RUNNING.

17. (original) The method of claim 11, further comprising copying the task queue and the task table from the local memory of the given sub-processing unit into the shared memory when the given sub-processing unit has completed its use thereof.

18. (previously presented) The method of claim 17, further comprising: locking the task table prior to copying from the shared memory to the local memory of the given sub-processing unit, and unlocking the task table when the given sub-processing unit has completed its use thereof.

19. (currently amended) A method of managing processor tasks in a multi-processor computing system, comprising:

storing the processor tasks in a shared memory that is accessible by a plurality of processing units of the multi-processor computing system;

storing a task table in the shared memory, the task table including a task table entry associated with each of the processor tasks;

copying the task table from the shared memory to local memory of a given one of the processing units;

linking at least some of the task table entries together to achieve at least one list of processor tasks in hierarchical order;

at least initiating execution a first one of the processor tasks of the list within ~~a~~ the given one of the processing units, wherein the first one of the processor tasks yields the given processing unit such that it is capable of executing another of the processor tasks;

determining which of the other processor tasks should be executed next within the given processing unit by permitting the given processing unit to use the task table to make such determination;

modifying the task table entry for the first one of the processor tasks that yields to another one of the processor tasks; and

writing the task table back from local memory of the given processing unit to the shared memory;

wherein each of the task table entries includes at least one of: (i) an indication as to whether the associated processor task is ready to be executed by one or more of the processing units; (ii) an indication as to a priority level of the associated processor task; (iii) a pointer to a previous task table entry in a list of task table entries (a previous pointer); and (iv) a pointer to a next task table entry in the list of task table entries.

20. (previously presented) The method of claim 19, further comprising:

storing a task queue in the shared memory, the task queue including at least one of a head pointer and a tail pointer, the head pointer providing an indication of a new first one of the processor tasks in the list of processor tasks, and the tail pointer providing an indication of a last one of the processor tasks in the list of processor tasks; and

permitting the processing units to use the task table and the task queue to determine which of the processor tasks should be executed next.

21. (original) The method of claim 20, wherein the plurality of processing units include a plurality of sub-processing units, each of the sub-processing units having local memory, and wherein the step of determining includes:

copying the task queue and the task table from the shared memory into a local memory of the given sub-processing unit; and

searching the task queue for the head pointer to the new first processor task that is ready to be invoked.

22. (original) The method of claim 20, further comprising: adding the first processor task back into the list.

23. (original) The method of claim 22, wherein:

each of the task table entries includes a pointer to a next task table entry and pointer to a previous task table entry; and

the step of adding includes modifying the linking of the task table entries to include links to the task table entry associated with the first processor task.

24. (original) The method of claim 23, wherein the step of modifying the linking of the task table entries includes linking the task table entry associated with the first processor task between a prior task table entry and a following task table entry that were previously linked to one another.

25. (original) The method of claim 24, further comprising:

modifying the next pointer of the prior task table entry to point to the task table associated with the first processor task;

modifying the previous pointer of the task table entry associated with the first processor task to point to the prior task table entry;

modifying the next pointer of the task table entry associated with the first processor task to point to the following task table entry; and

modifying the previous pointer of the following task table entry to point to the task table entry associated with the first processor task.

26. (currently amended) A multi-processor apparatus, comprising:

a plurality of processing units, each processing unit including a local memory in which to execute processor tasks;

a shared memory configured to store processor tasks that are ready to be executed, and

a task table including a task table entry associated with each of the processor tasks;

wherein the processing units are configured to determine which of the processor tasks should be executed based on priorities of the processor tasks, the processor tasks that are executed are copied from the shared memory to the local memory of a respective one of the plurality of processing units prior to execution, and

wherein the respective processing unit is configured to copy the task table from the shared memory to the local memory of the respective processing unit ~~and is configured,~~ to modify the task table entry of a given one of the processor tasks selected for execution, to link at least some of the task table entries together to achieve at least one list of the processor tasks to be invoked in hierarchical order, and to copy the task table, including the modified task table entry, from the local memory to the shared memory.

27. (cancelled)

28. (original) The apparatus of claim 26, wherein the plurality of processing units comprise a main processing unit and a plurality of sub-processing units and the sub-processor units access the processor tasks in the shared memory.

29. (currently amended) A multi-processor apparatus, comprising:

a plurality of processing units, each processing unit including a local memory in which to execute processor tasks; and

a shared memory configured to store: (i) processor tasks that are ready to be executed, and (ii) a task table including a task table entry associated with each of the processor tasks,

wherein the processing units are configured to copy the task table from shared memory to local memory, to use the task table to determine which of the processor tasks should be copied from the shared memory into their local memories and executed, ~~and are configured~~ to maintain and modify the task table during execution of the processor tasks, and to copy the modified task table from the local memory to the shared memory, and

wherein at least some of the task table entries are linked together to achieve at least one list of processor tasks to be invoked in hierarchical order, and the processing units are configured to use the linked list to determine which of the processor tasks should be copied from the shared memory and executed.

30. (cancelled)

31. (currently amended) The apparatus of claim [30]29, wherein each of the task table entries includes at least one of: (i) an indication as to whether the associated processor task is ready to be executed by one or more of the sub-processing units; (ii) an indication as to a priority level of the associated processor task; (iii) a pointer to a previous task table entry in the list of task table entries; and (iv) a pointer to a next task table entry in the list of task table entries.

32. (currently amended) The apparatus of claim [30]29, wherein:

the shared memory is further configured to store a task queue having at least one of a head pointer and a tail pointer, the head pointer providing an indication of a first one of the processor tasks in the list of processor tasks, and the tail pointer providing an indication of a last one of the processor tasks in the list; and

the processing units are configured to use the task table and the task queue to determine which of the processor tasks should be executed in accordance with the list of processor tasks.

33. (previously presented) The apparatus of claim 32, wherein the processor tasks that are executed are copied from the shared memory to the local memories of the processing units prior to execution.

34. (original) The apparatus of claim 32, wherein:

respective groups of the task table entries are linked together to produce respective lists of processor tasks, each list being in hierarchical order; and

the task queue includes respective task queue entries, each entry including at least one of a head pointer and a tail pointer for each of the lists of processor tasks.

35. (original) The apparatus of claim 34, wherein:

each of the respective lists are associated with processor tasks of a common priority level; and

the task queue includes a task queue entry for each of a plurality of priority levels of the processor tasks.

36. (previously presented) The apparatus of claim 32, wherein the plurality of processing units includes a plurality of sub-processing units, each of the sub-processing units having local memory, the sub-processing units are configured to:

copy the task queue and the task table from the shared memory into their respective local memories;

search the task queue for the head pointer to a given one of the processor tasks that is ready to be invoked; and

copy the given processor task from the shared memory to the local memory thereof for execution.

37. (previously presented) The apparatus of claim 36, wherein the sub-processing units are configured to search the task queue for the head pointer to a highest priority level one of the processor tasks that is ready to be invoked.

38. (previously presented) The apparatus of claim 36, wherein the sub-processing units are configured to remove the given processor task from the list.

39. (previously presented) The apparatus of claim 38, wherein:

each of the task table entries includes a pointer to a next task table entry; and

the sub-processing units are configured to modify the head pointer to identify the new first processor task as being ready to be next invoked using the next pointer of the given task table entry.

40. (previously presented) The apparatus of claim 38, wherein:

each of the task table entries includes a pointer to a previous task table entry; and

the sub-processing units are configured to modify the previous pointer of the last task table entry of the list to point to the task table entry associated with the new first processor task of the list.

41. (previously presented) The apparatus of claim 36, wherein:

each of the task table entries includes an indication as to whether the associated processor task is READY to be executed or is RUNNING on one or more of the sub-processing units; and

the sub-processing units are configured to modify the given task table entry to indicate that the given processor task is RUNNING.

42. (previously presented) The apparatus of claim 36, wherein the sub-processing units are configured to copy the task queue and the task table from the local memory thereof into the shared memory when the given sub-processing unit has completed its use thereof.

43. (currently amended) A multi-processor apparatus, comprising:

a plurality of sub-processing units, each sub-processing unit including a local memory in which to execute processor tasks; and

a shared memory configured to store: (i) processor tasks that are ready to be executed, and (ii) a task table including a task table entry associated with each of the processor tasks, wherein:

the sub-processing units are configured to at least initiate execution a first processor task and yield such that it is capable of executing another of the processor tasks,

the sub-processing units are configured to determine which of the other processor tasks should be executed next based on the task table,

each sub-processing unit is configured to copy the task table from the shared memory to its local memory,

the sub-processing units are configured to modify the task table entry for the first one of the processor tasks that yields to another one of the processor tasks, and

~~the~~ each sub-processing unit~~s are~~ is configured to write the task table back from ~~the~~ it's local memory ~~of the given processing unit~~ to the shared memory;

wherein at least some of the task table entries are linked together to achieve at least one list of processor tasks in hierarchical order.

44. (cancelled)

45. (currently amended) The apparatus of claim [44]43, wherein:

the shared memory is configured to store a task queue having at least one of a head pointer and a tail pointer, the head pointer providing an indication of a new first one of the processor tasks in the list of processor tasks, and the tail pointer providing an indication of a last one of the processor tasks in the list; and

the sub-processing units are configured to use the task table and the task queue to determine which of the processor tasks should be executed next.

46. (previously presented) The apparatus of claim 45, wherein the sub-processing units are configured to:

copy the task queue and the task table from the shared memory into the local memory thereof; and

search the task queue for the head pointer to the new first processor task that is ready to be invoked.

47. (previously presented) The apparatus of claim 45, wherein the sub-processing units are configured to add the first processor task back into the list.

48. (previously presented) The apparatus of claim 47, wherein:

each of the task table entries includes a pointer to a next task table entry and pointer to a previous task table entry; and

the sub-processing units are configured to modify the linking of the task table entries to include links to the task table entry associated with the first processor task.

49. (previously presented) The apparatus of claim 48, wherein the sub-processing units are configured to modify the linking of the task table entries by linking the task table entry associated with the first processor task between a prior task table entry and a following task table entry that were previously linked to one another.

50. (previously presented) The apparatus of claim 49, wherein the sub-processing units are configured to:

modify the next pointer of the prior task table entry to point to the task table associated with the first processor task;

modify the previous pointer of the task table entry associated with the first processor task to point to the prior task table entry;

modify the next pointer of the task table entry associated with the first processor task to point to the following task table entry; and

modify the previous pointer of the following task table entry to point to the task table entry associated with the first processor task.

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDULLAH AL KAWSAR whose telephone number is (571)270-3169. The examiner can normally be reached on 7:30am to 5:00pm, EST.

6. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng Ai T. An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

/Abdullah-Al Kawsar/
Examiner, Art Unit 2195